CLAIMS

What is claimed is:

1. A layout of a programmable logic device comprising a plurality of configurable function generators (CFG) and storage elements, said layout comprising:

a plurality of blocks, each block comprising a plurality of CFGs and storage elements, said blocks paired to a first adjacent block that is adjacent in a first direction and a second adjacent block that is adjacent in a second direction;

a first block connector tab network coupled to each block of the plurality of blocks that programmably couples in the first direction the CFGs of the block to routing lines of the device and a second block connector tab network coupled to each block of the plurality of blocks that programmably couples in the second direction the CFGs of the block to routing lines of the device, the first and second block connector tab networks of paired blocks oriented to mirror images of each other, each of said first and second said block connector tab networks comprising a memory and passgate array for forming a plurality of programmable connections and driver logic for driving signals, the memory and passgate arrays of paired blocks combined into a single array; and

a turn network for programmably coupling routing lines, said turn network comprising a memory and passgate array, said memory and passgate array of the turn network contiguous to the memory and passgate arrays of the first block connector tab networks and second block connector tab networks.

2. The layout as set forth in claim 38, wherein a block comprises a plurality of logic clusters, each logic cluster comprising a set of the plurality of CFGs and storage elements programmably interconnected via a cluster routing matrix composed of intracluster routing lines and programmable switches, a layout within each block comprising:

a memory and passgate array comprising;

a first portion comprising memory and passgates corresponding to switches of the cluster routing matrix of each logic cluster of the block;

a second portion comprising memory and passgates corresponding to switches of extensions which programmably couples cluster routing matrices of adjacent clusters within the block;

a third portion comprising memory and passgates corresponding to switches which programmably couple CFGs to block connectors, said block connectors programmably coupled to the block connector tab networks; and

a plurality of logic arrays, each logic array corresponding to the CFGs of a cluster, said logic arrays located external to the area spanned by the memory and passgate array.